

**S/N Unknown**

**PATENT**

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicant: Kie Y. Ahn et al.

Examiner: Unknown

Serial No.: Unknown

Group Art Unit: Unknown

Filed: Herewith

Docket: 303.678US3

Title: STRUCTURE AND METHOD FOR DUAL GATE OXIDE THICKNESSES

**PRELIMINARY AMENDMENT**

BOX PATENT APPLICATION

Commissioner for Patents

Washington, D.C. 20231

Sir:

Prior to taking up the above-identified patent application for examination, please amend the application as follows:

**IN THE SPECIFICATION**

On page 1, line 3, before the heading, "Field of the Invention", insert the following paragraph:

**Cross Reference to Related Application(s)**

This application is a division of U.S. Patent Application No. 09/514,629, filed on February 28, 2000, the specification of which is incorporated herein by reference.

**IN THE CLAIMS**

Please cancel claims 1 - 32 and 41 - 54, without prejudice or disclaimer, after adding the following new claims.

- Sub 12  
11.2
55. (New) A logic device and a memory device structure on a single substrate, comprising:  
a first transistor, wherein the first transistor includes:  
a first dielectric layer of a first thickness less than 5 nanometers (nm);  
a top layer which exhibits a high resistance to oxidation at high temperatures; and  
a second transistor, wherein the second transistor includes a second dielectric layer of a second thickness.